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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,025	01/20/2004	Junji Oohara	01-542	7090
23400	7590	12/08/2005	EXAMINER	
POSZ LAW GROUP, PLC			PE, MARK D	
12040 SOUTH LAKES DRIVE			ART UNIT	PAPER NUMBER
SUITE 101				
RESTON, VA 20191			2811	

DATE MAILED: 12/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/759,025	OOHARA ET AL.	
	Examiner Mark D. Pe	Art Unit 2811	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 04 October 2005.
- 2a) This action is FINAL.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-36 is/are pending in the application.
  - 4a) Of the above claim(s) 1-19 is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 20-22,28-32,34 and 35 is/are rejected.
- 7) Claim(s) 23-27 and 32,33,36 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 20 January 2004 is/are: a) accepted or b) objected to by the Examiner.
 

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    - a) All    b) Some \* c) None of:
      1. Certified copies of the priority documents have been received.
      2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
      3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 20040120.
- 4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: \_\_\_\_\_.

## DETAILED ACTION

### ***Election/Restrictions***

1) Applicant's election of group II (claims 20-36) in the reply filed on 10/04/2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

### ***Claim Objections***

2) Claim 29 objected to because of the following informalities:

To better comprehend the claims please do the following:

In line 2, replace "including" with -- includes --.

In line 4, replace "with using the" with -- using a --.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3) Claim 32 and 36 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

**Claim 32** recites the limitation "a film thickness direction" in line 4-5. There is insufficient antecedent basis for this limitation in the claim.

**Claim 36** recites the limitation "the epitaxial layer" in line 1. There is insufficient antecedent basis for this limitation in the claim.

***Claim Rejections – 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4) Claims 20-22 and 28-31 rejected under 35 U.S.C. 102(b) as being anticipated by MacDonald et al. (US 5628917) in figures 1a-1n, 5b, 6 and 7a/7b.

**With respect to claim 20,** MacDonald et al. discloses, "A method for manufacturing an optical device, comprising the steps of:

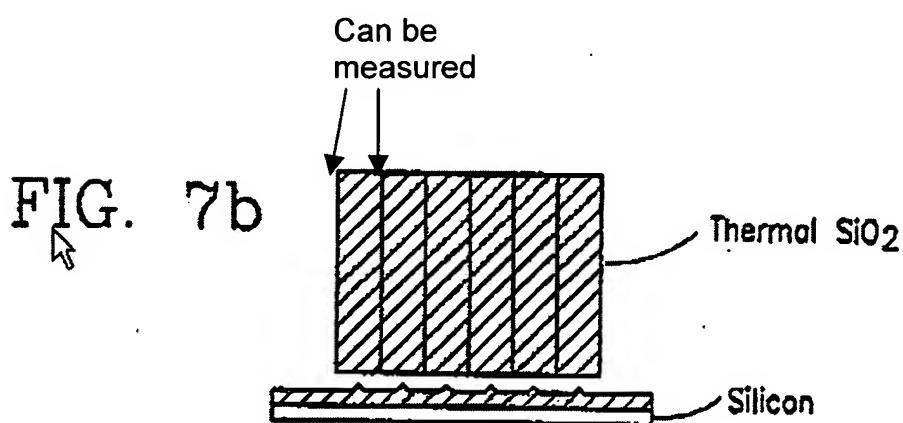
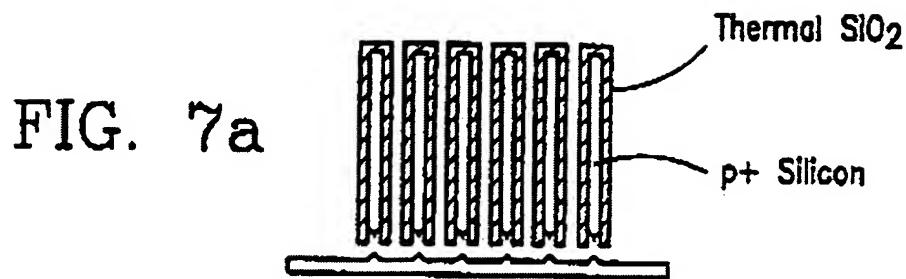
etching a semiconductor substrate with a predetermined mask (14) so that a plurality of semiconductor wall is formed between the trenches (see Figure 7a); and thermally oxidizing the substrate so that the semiconductor wall is transformed into a semiconductor oxide wall (thermal SiO<sub>2</sub>; Oxidation discussed also in Figure 5b; Col. 7: lines 35-42; Col. 5: lines 52-58) and the trench is filled with semiconductor oxide (see Figure 7b),

wherein the semiconductor oxide wall and the semiconductor oxide in the trench provide an optical part (light waveguide 168 in Figure 6), and

wherein the optical part is integrally formed with the substrate (10), and passes light therethrough.

**With respect to claim 21,** MacDonald et al. further discloses, " wherein the semiconductor substrate is made of silicon (Col. 5: lines 19-22), and wherein the optical part is made of silicon oxide (See Figure 7b), wherein the semiconductor oxide wall (thermal SiO<sub>2</sub> in figure 7a) and the semiconductor oxide in the trench are adhered together in the step of thermally oxidizing the substrate (see Figure 7b: Col. 7: lines 59-61)."

**With respect to claim 22,** MacDonald et al. further discloses, "wherein the trench has a width, and the semiconductor wall has another width, and wherein the widths of both of the trench of the semiconductor wall are determined (can be measured) in such a manner that the trench is filled with the semiconductor oxide and at the same time the semiconductor wall is transformed into the semiconductor wall in the step of thermally oxidizing the substrate (see figure 7a and 7b below)."



**With respect to claim 28,** MacDonald et al. further discloses, "wherein each trench is parallel to an optical axis of the optical part (as seen on Figure 6: 168; waveguide parallel to an axis of Figure 7a or Figure 7b)."

**With respect to claim 29,** MacDonald et al. further discloses, " wherein the step of etching the substrate including the steps of:

etching the substrate with using reactive ion etching method (Col. 5: 38-45) so that the initial trench is formed;

forming a passivation oxide film (18) in an inner wall of the initial trench (Figure 1f: 18);

etching the passivation oxide film (Fig. 1g) disposed on a bottom of the initial trench; and

etching the bottom of the initial trench with using the reactive ion etching method so that a final trench having a high ratio is formed (Col. 5 lines 65-67 and Col. 6: lines 1-16 and 40-48)."

**With respect to claim 30,** MacDonald et al. further discloses, "wherein the optical part includes at least one of a lens, a light guide or a slit so that the optical part is integrally formed with the substrate (Figure 7a and Figure 7b – light wave guide - 168)."

**With respect to claim 31,** MacDonald et al. further discloses, "wherein the step of thermally oxidizing the substrate further includes the step of:

depositing (growing) a semiconductor oxide film in a clearance in the trench (as shown in Figure 7a) in a case where the trench has a clearance after the semiconductor oxide is formed on a sidewall of the trench in the step of thermally oxidizing the substrate (Col 7: lines 56-61)."

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5) Claims 34-35 rejected under 35 U.S.C. 103(a) as being unpatentable over MacDonald et al. (US 5628917) in view of Strain (US 4585299).

**With respect to claim 34,** MacDonald was silent on further comprising the steps of:

implanting an impurity on the substrate so that an impurity doped layer is formed, wherein the impurity doped layer includes an impurity concentration distribution having a chevron shape in a film thickness direction.

Strain teaches implanting the substrate with an impurity (Figure 1e; Col. 4: lines 41-44) dope concentration distribution (concentration distribution is inherent in doping impurities – there is always a concentration distribution within the area of doping) with a rectangular shape in Figures 1d and 1e on the substrate. Strain also shows this as a polygon in Figure 2b (18; Col 4 lines: 25-44) to form the impurity doped layer. The chevron shape in a film thickness direction is just a change in shape and is not patentable over the prior art's rectangular and/or polygon shape. See *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Strain with MacDonald et al. to dope an impurity concentration onto the substrate (any shape needed) to increase the index of refraction of the core or interior region compared to the surrounding silicon dioxide to confine the light energy within a region approximately 1 micron from the core and the silicon concentration will increase the index of refraction to the desired extent (Col. 2: lines 23-37).

**With respect to claim 35,** MacDonald et al. was silent on further comprising the step of:

annealing the substrate in a dopant atmosphere so that an impurity doped layer is formed,

wherein the impurity doped layer includes an impurity concentration distribution having a chevron shape in a film thickness direction.

Strain teaches annealing (oxidizing: Col. 4: lines 45-61) the substrate in a dopant atmosphere with an impurity dope concentration distribution (Figure 1e; Col. 4: lines 41-44; concentration distribution is inherent in doping impurities – there is always a concentration distribution within the area of doping) with a rectangular shape in Figures 1d and 1e on the substrate. Strain also shows this as a polygon in Figure 2b (18; Col 4 lines: 25-44) to form the impurity doped layer. The chevron shape in a film thickness direction is just a change in shape and is not patentable over the prior art's rectangular and/or polygon shape. See *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Strain with MacDonald et al. to attain the doped layer (any shape as needed) upon doping then annealing the substrate in a dopant atmosphere (oxidation) to increase the index of refraction of the core or interior region compared to the surrounding silicon dioxide to confine the light energy within a region approximately 1 micron from the core and the silicon concentration will increase the index of refraction to the desired extent (Col. 2: lines 23-37).

***Allowable Subject Matter***

6) Claims 23-27 and 32, 33, 36 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: The prior art does not teach forming a plurality of trenches formed in the substrate and a plurality of semiconductor wall is formed in the trenches; and thermally oxidizing the substrate so that the semiconductor wall is transformed into a semiconductor oxide wall and the trench is filled with semiconductor oxide, wherein the semiconductor wall and the semiconductor oxide provide an optical part, and wherein the optical part is integrally formed with the substrate and passes light therethrough and wherein the width of both the trench and the semiconductor oxide wall are determined in such a manner that the trench is filled with the semiconductor oxide and at the same time the semiconductor wall is transformed into the semiconductor oxide wall in the step of thermally oxidizing the substrate in combination with claims 23-27 and 32, 33, 36.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

7) Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark D. Pe whose telephone number is (571)272-8780. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571)272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MDP



GEORGE ECKERT  
PRIMARY EXAMINER